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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,991	05/02/2001	Jason Seung-Min Kim	2100653-991140	5788
7590	11/09/2005		EXAMINER	
DAVID H. JAFFER PILLSBURY WINTHROP LLP 2475 HANOVER STREET PALO ALTO, CA 94304-1114			MYERS, PAUL R	
			ART UNIT	PAPER NUMBER
			2112	

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,991	KIM ET AL.	
	Examiner Paul R. Myers	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 29 August 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-27 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/4/05.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/29/05 have been fully considered but they are not persuasive.

In regards to applicants argument that MacLellan is not relevant to the presently claimed invention: This is clearly incorrect. MacLellan discloses a computer system (100) having a multipath cross bar bus (crossbar 260), comprising: one or more processors (121); one or more resources (memory 220 or disk drives 140) capable of being shared by the one or more processors; and a resource controller (controller 260) and bus that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous accesses; col. 14, lines 35-40, 57 to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 to col. 21, lines 1-2).

In regards to applicants argument that MacLellan teaches away from a hardware semaphore unit: This is clearly incorrect. The examiner has been unable to find any teachings in MacLellan stating that it would be disadvantageous to use a hardware semaphore.

In regards to applicants argument that nowhere does MacLellan teach a resource controller including a hardware semaphore unit for controlling access to a shared resource: The examiner agrees. The rejection however is MacLellan in view of Holt. Holt et al PN 5,394,551 teaches each node includes a semaphore unit 22 which controls access to the shared resource 21, a semaphore ownership table 24 and a semaphore queue 25.

In regards to applicants argument that MacLellan does not teach a hardware semaphore unit for prioritizing access to the set of memory resources as required in claim 27: The rejection is MacLellan in view or Holt further in view of what is well known in the art as evidenced by Dhuey. The way a semaphore works is the device that sets the semaphore has priority to the shared resource associated with the semaphore. Thus the semaphores of Holt prioritize access to the memory resources. The claim language does not state that the memory resources are given higher priority than other resources, or that they are given lower priority, or how they are prioritized only that they are prioritized.

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. *In re Nomiya*, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. *In re McLaughlin*, 170 USPQ 209 (CCPA 1971). references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. *In re Bozek*, 163 USPQ 545 (CCPA) 1969. Holt teaches a semaphore unit. It is understood that a semaphore is to prevent contention for a shared resource. MacLellan teaches accessing shared resources. Thus it would have been obvious to include Holt's semaphore mechanism in the system of MacLellan because this would have been a simple way of preventing contention for the shared resources.

In regards to applicants argument that Holt does not teach a hardware semaphore unit: This is incorrect. Holt's semaphore unit is expressly a mechanism/unit. However for the sake of argument hardware and software are logically equivalent. Thus, even if Holt's did not expressly state the semaphore was a mechanism/unit. It would have been obvious to a person of ordinary skill in the art to use a hardware semaphore in the system of MacLellan in view of Holt because this would have provided for one of the well known purposes of using hardware (such as hardware is faster than software).

In regards to applicants argument that Srini never mentions the use of semaphores: The examiner agrees. The rejection however is Srini in view of Holt which teaches the hardware semaphore as described above. Srini does teach an arbiter to prevent contention of access to a resource that is identified for connection to another processor. Srini does not state how it knows which resource is in use. Preventing contention is the purpose of a semaphore that indicates which resource is in use.

In regards to applicants argument that Goodwin never mentions the use of semaphores: The examiner agrees. The rejection however is Goodwin in view of Holt which teaches the hardware semaphore as described above. Goodwin does teach an arbiter to prevent contention of access to a resource that is identified for connection to another processor. Goodwin does not state how it knows which resource is in use. Preventing contention is the purpose of a semaphore that indicates which resource is in use.

In regards to applicants argument that Hiller never mentions the use of semaphores: The examiner agrees. The rejection however is Hiller in view of Holt which teaches the hardware semaphore as described above. Hiller also states that normally two processing elements cannot

access the same memory module at the same time. Two processing elements trying to access the same memory at the same time is called contention. Hiller does not state how it knows which resource is in use. Preventing contention is the purpose of a semaphore that indicates which resource is in use.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 8-9, 11-13, 18-19, 21-22, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacLellan et al PN 6,636,933 in view of Holt et al PN 5,394,551.

As per claims 1,11, and 21, MacLellan discloses a computer system (100) having a multipath cross bar bus (crossbar 260), comprising: one or more processors (121); one or more resources (memory 220 or disk drives 140) capable of being shared by the one or more processors; and a resource controller (controller 260) and bus that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (crossbar switch

system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous accesses; col. 14, lines 35-40, 57 to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 to col. 21, lines 1-2). MacLellan also teaches semaphores for signaling however MacLellan is silent as to how the Semaphores are to be implemented. Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource.

As per claims 2 and 12, MacLellan discloses memory resources (plural global memory boards 220; col. 12, lines 41+; Fig. 8; col. 14, lines 12+ to col. 15, lines 1+); memory controller (logic sections e.g. 5010; col. 18, lines 42-55);

As per claims 3, 13 and 22, MacLellan discloses crossbar switches 5004 (col. 18, lines 5+); and resource arbitration controller (fig. 10; col. 19, lines 11+; col. 23, lines 26+);

As per claims 8, 18 and 24, MacLellan discloses a plurality of peripheral resources (plural disks drives 140); and peripheral controller (switch controller 260) wherein the controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2).

As per claims 9, 19 and 25, MacLellan discloses crossbar switches 5004 (col. 18, lines 5+); and resource arbitration controller (fig. 10; col. 19, lines 11+; col. 23, lines 26+).

4. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacLellan et al PN 6,636,933 in view of Holt et al PN 5,394,551 as applied to claim 1 above and further in view of Official Notice as evidenced by Dhuey et al PN 5,805,030.

As per claim 27, MacLellan discloses a computer system (100; fig. 1) comprising: a first processor (121₁); a second processor (121₂); a multipath memory controller (controller 260) having a first bus that is capable of connecting the first processor to a set of memory resources and a second bus that is capable of connecting the second processor to the same set of memory resources wherein the first and second processors are capable of simultaneously accessing different memory resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2); a multipath peripheral controller (controller 260) having a first bus that is capable of connecting the first processor to a set of peripheral resources (disk drives) and a second bus that is capable of connecting the second processor to the same set of peripheral resources (disk drives) wherein the first and second processors are capable of simultaneously accessing different peripheral resources (crossbar switch system interface 160 allows simultaneous accesses to different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2). Holt et al teaches each resource of a plurality of shared resources has a semaphore

which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource. MacLellan in view of Holt teaches a single resource controller with semaphores for each resource. Official Notice is taken that to have separate Memory controller and Peripheral controllers is well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of the invention to have separate memory and peripheral controllers because this would have allowed for faster concurrent access processing of different types of resources. See also MPEP 2144.04 V. C.

5. Claims 1-3 are rejected under 35 U.S.C. 103(b) as being unpatentable over Srini (USPN 5,053,942) in view of Holt et al PN 5,394,551.

As per claim 1, Srini discloses a computer system (e.g. Fig. 1) having a multipath cross bar bus (crossbar matrix 20), comprising: one or more processors (12); one or more resources (memory 22) capable of being shared by the one or more processors (12); and a resource controller (crossbar chip 10) and bus (26) that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 8, lines 30-50). Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the

respective resources because this would have prevented multiple concurrent accesses of the same shared resource.

As per claim 2, Srini discloses memory resources (plural memory modules 22; col. 4, lines 15+); memory controller (arbiter 18 and logic; col. 4, lines 41-51);

As per claim 3, Srini discloses crossbar switches 20; and resource arbitration controller (arbiter 18; col. 4, lines 41+)

6. Claims 1-3, 8-9, 11-13, 18-19, 21-22 and 24-25 are rejected under 35 U.S.C. 103(e) as being unpatentable over Goodwin et al. (USPN 6,125,429; Goodwin) in view of Holt et al PN 5,394,551.

As per claims 1, 11 and 24, Goodwin discloses a computer system (e.g. Fig. 1) having a multipath crossbar bus (crossbar 12), comprising: one or more processors (CPU0 to CPU3); one or more resources (memory M0-M3 or I/O 16) capable of being shared by the one or more processors (CPU0-CPU3); and a resource controller (arbitor 14) and bus that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 2, lines 46-52; col. 4, lines 26-36; 49-62). Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource.

As per claims 2, 8, 12, 18 and 25, Goodwin discloses memory or peripheral resources (plural memory modules M0-M3; col. 4, lines 26+; or I/O 16); memory or peripheral controller (arbiter chip 14; col. 4, lines 61+);

As per claims 3, 9, 13 and 19, Goodwin discloses crossbar switches 12; and resource arbitration controller (arbiter 14; col. 4, lines 26+)

As per claim 21, Goodwin discloses an apparatus for controlling the access to one or more memory resources by one or more processors, the controller comprising a memory resource controller (arbiter 14) and bus (crossbar switch) that is connected to each memory resource and to each processor so wherein the memory resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more memory resources (col. 2, lines 45-52; col. 4, lines 26-36; 49-62).

As per claim 22, Goodwin discloses crossbar switches 12; and resource arbitration controller (arbiter 14; col. 4, lines 26+)

7. Claim 27 is rejected under 35 U.S.C. 103(e) as being unpatentable over Goodwin et al. (USPN 6,125,429; Goodwin) in view of Holt et al PN 5,394,551 as applied to claim 1 above and further in view of Official Notice as evidenced by Dhuey et al PN 5,805,030

As per claim 27, Goodwin discloses a computer system (10; fig. 1) comprising: a first processor (20); a second processor (22); a multipath memory controller (arbiter 14 and x-bar switch 12) having a first bus that is capable of connecting the first processor to a set of memory resources and a second bus that is capable of connecting the second processor to the same set of memory resources wherein the first and second processors are capable of simultaneously

accessing different memory resources (col. 2, lines 45-52; col. 4, lines 26-36; 49-62); a multipath peripheral controller (arbitor 14 and x-bar switch 12) having a first bus that is capable of connecting the first processor to a set of peripheral resources and a second bus that is capable of connecting the second processor to the same set of peripheral resources wherein the first and second processors are capable of simultaneously accessing different peripheral resources (col. 2, lines 45-52; col. 4, lines 26-36; 49-62). Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource. Goodwin in view of Holt teaches a single resource controller with semaphores for each resource. Official Notice is taken that to have separate Memory controller and Peripheral controllers is well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of the invention to have separate memory and peripheral controllers because this would have allowed for faster concurrent access processing of different types of resources. See also MPEP 2144.04 V. C.

8. Claims 1-2, 11-12, 21 and 24 are rejected under 35 U.S.C. 103(b) as being unpatentable over Hiller et al. (USPN 5,081,575; Hiller) in view of Holt et al PN 5,394,551.

As per claims 1, 11 and 24, Hiller discloses a computer system (e.g. Fig. 1) having a multipath crossbar bus (crossbar 6), comprising: one or more processors (PEs); one or more resources (PMEMs 8) capable of being shared by the one or more processors (PEs); and a resource controller (control section) and bus (crossbar bus) that is connected to each resource and

to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (e.g. col. 6, lines 55-57). Holt et al teaches each resource of a plurality of shared resources has a semaphore which controls access to the shared resource (Column 2 lines 59-68). It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a semaphore for the respective resources because this would have prevented multiple concurrent accesses of the same shared resource.

As per claims 2 and 12, Hiller discloses memory (PMEMs 8); memory controller (control section; col. 6, lines 55 et seq).

As per claim 21, Hiller discloses an apparatus for controlling the access to one or more memory resources (PMEMs) by one or more processors (PEs), the controller comprising a memory resource controller (control section; col. 6, lines 55 et seq) and bus (crossbar switch) that is connected to each memory resource and to each processor so wherein the memory resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more memory resources (col. 6, lines 55-57).

9. Claims 3-4, 13-14, 22-23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable Hiller et al. (USPN 5,081,575; Hiller) in view of in view of Holt et al PN 5,394,551 as applied to claim 1 above and further in view of Goodwin et al. (USPN 6,125,429; Goodwin).

As per claims 3, 13, 23 and 25; Hiller discloses crossbar switch 6. However, Hiller does not teach an arbitration controller. Goodwin teaches that it is known to use a resource arbitration controller to resolve contentions or collisions in a computer system using a crossbar switch (col.

2, lines 30-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hiller and Goodwin as taught by Goodwin to include a resource arbitration controller in a crossbar switch type system such as that of Hiller to resolve the collisions and contentions particularly in bus systems such as that of Hiller with large numbers of data users (PEs) and resources (PMEMs) connected to them (col. 2, lines 55-67).

As per claims 4, 14, 23 and 26, Hiller teaches that the crossbar switch comprises multiplexer (col. 6, lines 57-64).

10. Claims 4-7, 10, 14-17, 20, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable MacLellan et al (USPN 6,636,933; MacLellan) in view of Holt et al PN 5,394,551 as applied to claim 1 above and further in view of Official Notice as evidenced by Hiller et al. (USPN 5,081,575; Hiller).

As per claims 4, 7, 10, 14, 17, 20, 23, and 26, MacLellan teaches all the limitations of the claimed invention including crossbar switch. However, MacLellan is silent as to the switch comprise multiplexer. Official Notice is taken that crossbar switch comprise a multiplexer is notoriously well known in the crossbar switch art at the time the invention was made such as evidenced by Hiller in that multiplexer is utilized in crossbar switch do perform actual switching of signal paths (bus) to connect pairs of processors and resources.

As per claims 5 and 15, MacLellan discloses a plurality of peripheral resources (plural disks drives 140); and peripheral controller (switch controller 260) wherein the controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources (crossbar switch system interface 160 allows simultaneous accesses to

different resources from different processors; parallel transfers or simultaneous transfers; col. 14, lines 35-40, 57 et seq. to col. 15, lines 1-5; col. 18, lines 50-53; col. 20, lines 58 et seq. to col. 21, lines 1-2).

As per claims 6 and 16, MacLellan discloses crossbar switches 5004 (col. 18, lines 5+); and resource arbitration controller (fig. 10; col. 19, lines 11+; col. 23, lines 26+);

11. Claims 4-7, 10, 14-17, 20, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodwin et al. (USPN 6,125,429; Goodwin) in view of Holt et al PN 5,394,551 as applied to claim 1 and further in view of Official Notice as evidenced by Hiller et al. (USPN 5,081,575; Hiller).

As per claims 4, 7, 10, 14, 17, 20, 23, and 26, Goodwin teaches all the limitations of the claimed invention including crossbar switch. However, Goodwin is silent as to the switch comprise multiplexer. Official Notice is taken that crossbar switch comprise a multiplexer is notoriously well known in the crossbar switch art at the time the invention was made such as evidenced by Hiller in that multiplexer is utilized in crossbar switch do perform actual switching of signal paths (bus) to connect pairs of processors and resources.

As per claims 5 and 15, Goodwin discloses memory or peripheral resources (plural memory modules M0-M3; col. 4, lines 26+; or I/O 16); memory or peripheral controller (arbiter chip 14; col. 4, lines 61+);

As per claims 6 and 16, Goodwin discloses crossbar switches 12; and resource arbitration controller (arbiter 14; col. 4, lines 26+)

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Microsoft Press Computer Dictionary: Definitions of Priority and Semaphore.

Structured Computer Organization: Shows that hardware and software are logically equivalent.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



PAUL R. MYERS
PRIMARY EXAMINER

PRM
November 7, 2005